WHAT IS CLAIMED IS:

1. A mixer, comprising:

a track and hold circuit to track and hold a first signal in response to a second signal; and

a bandpass circuit in cooperation with the track and hold circuit.

2. The mixer of claim 1 further comprising an input circuit to buffer the first signal before being applied to the track and hold circuit.

3. The mixer of claim 1 wherein the track and hold circuit comprises first and second output signals, the mixer further comprising a buffer to combine the first and second output signals.

4. The mixer of claim 1 wherein the bandpass circuit comprises an inductor and capacitor each being coupled to the track and hold circuit, the inductor and capacitor cooperating to provide a time constant related to a frequency of the first signal.

5. The mixer of claim 1 wherein the track and hold circuit comprises a switch in a path of the first signal, the switch being controlled by the second signal.

6. The mixer of claim 5 wherein the switch comprises a transistor having a gate coupled to the second signal.

7. The mixer of claim 6 wherein the transistor further comprises a source coupled to the first signal.

8. The mixer of claim of 7 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

9. The mixer of claim 8 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

10. The mixer of claim of claim 9 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

11. The mixer of claim of claim 7 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

12. The mixer of claim of 11 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

13. The mixer of claim of claim 12 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

14. The mixer of claim of 1 wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals.

15. The mixer of claim 14 wherein the track and hold circuit further comprises a first switch in a first path of a first one of the first differential signals and a second switch in a second path of the first one of the first differential signals, the first switch being controlled by a first one of the second differential signals and the second switch being controlled by a second one of the second differential signals.

16. The mixer of claim 15 wherein the track and hold circuit further comprises a third switch in a first path of a second one of the first differential signals and a fourth switch in a fourth path of the second one of the first differential signals, the third switch being controlled by the first one of the second differential signals and the fourth switch being controlled by a second one of the second differential signals.

17. The mixer of claim 16 wherein the first switch comprises a transistor having a gate coupled to the first one of the second differential signals, the second switch comprises a second transistor having a gate coupled to the second one of the second differential signals, the third switch comprises a third transistor having a gate coupled to the first one of the second differential signals, and the fourth switch comprises a fourth transistor having a gate coupled to the second one of the second differential signals.

18. The mixer of claim 17 wherein the transistors each further comprises a source, the sources of the first and second transistors each being coupled to the first one of the first differential signals and the sources of the third and fourth transistors each being coupled to the second one of the first differential signals.

19. The mixer of claim of 18 wherein the bandpass circuit comprises first, second, third and fourth capacitors, wherein the transistors each further comprises a drain, the drain of the first transistor being coupled to the first capacitor, the drain of the second transistor being coupled to the second capacitor, the drain of the third transistor being coupled to the third capacitor, and the drain of the fourth transistor being coupled to the fourth capacitor.

20. The mixer of claim of claim 19 wherein the bandpass circuit further comprises first and second inductors, the first inductor being coupled to the sources of the first and second transistors and the second inductor being coupled to the sources of the third and fourth transistors.

21. The mixer of claim of claim 20 further comprising an input circuit including fifth and sixth transistors each having a drain, the drain of the fifth transistor being coupled to the sources of the first and second transistors and the drain of the sixth transistor being coupled to the sources of the third and fourth transistors.

22. The mixer of claim of 18 wherein the first, second, third and fourth transistors each further comprises a drain, the mixer further comprising a buffer to convert voltages at the drains of the first and fourth transistors to a first current and voltages at the drains of the second and third transistors to a second current.

23. The mixer of claim 1 wherein the track and hold circuit comprises a transistor having an input adapted to be coupled to the first signal and an output to generate an output signal in response to the first signal, and a switch in a path of the output signal, the switch being controlled by the second signal.

24. The mixer of claim 23 wherein the switch comprises a second transistor having a gate coupled to the second signal.

25. The mixer of claim 24wherein the second transistor further comprises a drain coupled to the output of the transistor.

26. The mixer of claim of 25 wherein the bandpass circuit comprises a capacitor coupled to the output of the transistor.

27. The mixer of claim of 26 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

28. The mixer of claim of claim 27 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

29. The mixer of claim of 25 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

30. The mixer of claim of 29 wherein the bandpass circuit comprises a capacitor coupled to the output of the transistor.

31. The mixer of claim of claim 30 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

32. The mixer of claim of 1 wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals.

33. The mixer of claim 32 wherein the track and hold circuit comprises a first transistor having a first input adapted to be coupled to a first one of the first differential signals and a first output to generate a first output signal in response to the first one of the first differential signals, a second transistor having a second input adapted to be coupled to the first one of the first differential signals and a second output to generate a second output signal in response to the first one of the first differential signals, a third transistor having a third input adapted to be coupled to a second one of the first differential signals and a third output to generate a third output signal in response to the second one of the first differential signals, and a fourth transistor having a fourth input adapted to be coupled to the second one of the first differential signals and a fourth output to generate a fourth output signal

in response to the second one of the first differential signals, wherein the track and hold circuit further comprises a first switch in a path of the first output signal, a second switch in a path of the second output signal, a third switch in a path of the third output signal, and a fourth switch in a path of the fourth output signal, the first switch being controlled by a first one of the second differential signals, the second switch being controlled by a second one of the second differential signals, the third switch being controlled by the first one of the second differential signals, and the fourth switch being controlled by the second one of the second differential signals.

34. The mixer of claim 33 wherein the first switch comprises a fifth transistor having a gate coupled to the first one of the second differential signals, the second switch comprises a sixth transistor having a gate coupled to the second one of the second differential signals, the third switch comprises a seventh transistor having a gate coupled to the first one of the second differential signals, and the fourth switch comprises an eighth transistor having a gate coupled to the second one of the second differential signals.

35. The mixer of claim 34 wherein the bandpass circuit further comprising a first capacitor coupled to the first output of the first transistor, a second capacitor coupled to the second output of the second transistor, a third capacitor coupled to the third output of the third transistor, and a fourth capacitor coupled to the fourth output of the fourth transistor.

36. The mixer of claim of 35 wherein the fifth, sixth, seventh, and eighth transistors each comprises a drain and source, the drain of the fifth transistor being coupled to the first capacitor, the drain of the sixth capacitor being coupled to the second capacitor, the drain of the seventh transistor being coupled to the third capacitor, and the drain of the eighth transistor being coupled to the fourth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, a second inductor coupled to the drain of the sixth transistor, a third inductor coupled to the drain of the seventh transistor, and a fourth inductor coupled to the drain of the eighth transistor.

37. The mixer of claim of claim 36 wherein each of the first, second, third and fourth transistors comprises a source, the source of the first and third transistors being coupled together and the sources of the second and fourth transistors being coupled together, the mixer further comprising a fifth switch coupled to the common sources of the first and third transistors, and a sixth switch coupled to the common sources of the second and fourth transistors, the fifth switch being controlled

by the first one of the second differential signals and the sixth switch being controlled by the second one of the second differential signals.

38. The mixer of claim of 37 further comprising a buffer to convert voltages at the first and fourth outputs to a first current and voltages at the second and third outputs to a second current.

39. A mixer, comprising:

a track and hold circuit having a signal input, a control input, and a mixed signal output; and

a bandpass circuit coupled to the signal input and the mixed signal output.

40. The mixer of claim 39 further comprising an input circuit coupled to the signal input.

41. The mixer of claim 39 wherein the mixed signal output comprises first and second output signals, the mixer further comprising a buffer to combine the first and second output signals.

42. The mixer of claim 39 wherein the bandpass circuit comprises an inductor coupled to the signal input and a capacitor coupled to the mixed signal output.

43. The mixer of claim 39 wherein the track and hold circuit comprises a switch between the signal input and the mixed signal output, the switch being controlled by the control input.

44. The mixer of claim 43 wherein the switch comprises a transistor having a gate coupled to the control input.

45. The mixer of claim 44 wherein the transistor further comprises a source coupled to the signal input.

46. The mixer of claim of 45 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

47. The mixer of claim 46 wherein the bandpass circuit further comprises an inductor coupled to the signal input.

48. The mixer of claim of claim 47 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

49. The mixer of claim of claim 45 wherein the bandpass circuit further comprises an inductor coupled to the signal input.

50. The mixer of claim of 49 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

51. The mixer of claim of claim 50 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

52. The mixer of claim 39 wherein the track and hold circuit comprises a transistor having an input coupled to the signal input and an output coupled to the mixed signal output, and a current source coupled to the mixed signal output, the current source being controlled by the control input.

53. The mixer of claim 52 wherein the current source comprises a second transistor having a gate coupled to the control input.

54. The mixer of claim 53 wherein the second transistor further comprises a drain coupled to the mixed signal output.

55. The mixer of claim of 54 wherein the bandpass circuit comprises a capacitor coupled to the mixed signal output.

56. The mixer of claim of 55 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the drain of the second transistor.

57. The mixer of claim of claim 56 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

58. The mixer of claim of 55 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

59. The mixer of claim of 58 wherein the bandpass circuit comprises a capacitor coupled to the mixed signal output.

60. The mixer of claim of claim 59 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

61. A differential mixer, comprising:

a track and hold circuit having a differential signal input, a differential control input, and a differential mixed signal output; and

a bandpass circuit coupled to the differential signal input and the differential mixed signal output.

62. The mixer of claim 61 wherein the track and hold circuit further comprises a first switch between a first one of the differential inputs and a first one of the differential mixed signal outputs, and a second switch between the first one of the differential inputs and the first one of the differential mixed signal outputs, the first switch being controlled by a first one of the differential control inputs and the second switch being controlled by a second one of the differential control inputs.

63. The mixer of claim 62 wherein the track and hold circuit further comprises a third switch between a second one of the differential inputs and a second one of the differential mixed signal outputs, and a fourth switch between the second one of the differential inputs and the second one of the differential mixed signal outputs, the third switch being controlled by a first one of the differential control inputs and the fourth switch being controlled by a second one of the differential control inputs.

64. The mixer of claim 63 wherein the first switch comprises a transistor having a gate coupled to the first one of the differential control inputs, the second switch comprises a second transistor having a gate coupled to the second one of the differential control inputs, the third switch comprises a third transistor having a gate coupled to the first one of the differential control inputs, and the fourth switch comprises a fourth transistor having a gate coupled to the second one of the differential control inputs.

65. The mixer of claim 64 wherein the transistors each further comprises a source, the sources of the first and second transistors each being coupled to the first one of the differential signal inputs and the sources of the third and fourth transistors each being coupled to the second one of the differential signal inputs.

66. The mixer of claim of 65 wherein the bandpass circuit comprises first, second, third and fourth capacitors, wherein the transistors each further comprises a drain, the drain of the first transistor being coupled to the first capacitor, the drain of the second transistor being coupled to the second capacitor, the drain of the third transistor being coupled to the third capacitor, and the drain of the fourth transistor being coupled to the fourth capacitor.

67. The mixer of claim of claim 66 wherein the bandpass circuit further comprises first and second inductors, the first inductor being coupled to the sources of the first and second transistors and the second inductor being coupled to the sources of the third and fourth transistors.

68. The mixer of claim of claim 67 further comprising an input circuit including fifth and sixth transistors each having a drain, the drain of the fifth transistor being coupled to the sources of the first and second transistors and the drain of the sixth transistor being coupled to the sources of the third and fourth transistors.

69. The mixer of claim of 68 wherein the first, second, third, and fourth transistors each further comprises a drain, the mixer further comprising a buffer to convert voltages at the drains of the first and fourth transistors to a first current and voltages at the drains of the second and third transistors to a second current.

70. The mixer of claim 61 wherein the track and hold circuit comprises a first transistor having a first input coupled to a first one of the differential signal inputs and a first output, a second transistor having a second input coupled to the first one of the differential signal inputs and a second output, a third transistor having a third input coupled to a second one of the differential signal inputs, and a fourth transistor having a fourth input coupled to the second one of the differential signal inputs, wherein the track and hold circuit further comprises a first switch coupled to the first output, a second switch coupled to the second output, a third switch coupled to the third output, and a fourth switch coupled to the fourth output, the first switch being controlled by a first one of the differential control

inputs, the second switch being controlled by a second one of the differential control inputs, the third switch being controlled by the first one of the differential control inputs, and the fourth switch being controlled by the second one of the differential control inputs.

71. The mixer of claim 70 wherein the first switch comprises a fifth transistor having a gate coupled to the first one of the differential control inputs, the second switch comprises a sixth transistor having a gate coupled to the second one of the differential control inputs, the third switch comprises a seventh transistor having a gate coupled to the first one of the differential control inputs, and the fourth switch comprises an eighth transistor having a gate coupled to the second one of the differential control inputs.

72. The mixer of claim 71 wherein the bandpass circuit further comprising a first capacitor coupled to the first output of the first transistor, a second capacitor coupled to the second output of the second transistor, a third capacitor coupled to the third output of the third transistor, and a fourth capacitor coupled to the fourth output of the fourth transistor.

73. The mixer of claim of 72 wherein the fifth, sixth, seventh, and eighth transistors each comprises a drain and source, the drain of the fifth transistor being coupled to the first capacitor, the drain of the sixth capacitor being coupled to the second capacitor, the drain of the seventh transistor being coupled to the third capacitor, and the drain of the eighth transistor being coupled to the fourth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, a second inductor coupled to the drain of the sixth transistor, a third inductor coupled to the drain of the seventh transistor, and a fourth inductor coupled to the drain of the eighth transistor.

74. The mixer of claim of claim 73 wherein each of the first, second, third and fourth transistors comprises a source, the source of the first and third transistors being coupled together and the sources of the second and fourth transistors being coupled together, the mixer further comprising a fifth switch coupled to the common sources of the first and third transistors, and a sixth switch coupled to the common sources of the second and fourth transistors, the fifth switch being controlled by the first one of the differential control inputs and the sixth switch being controlled by the second one of the differential control input.

75. The mixer of claim of 74 further comprising a buffer to convert voltages at the first and fourth outputs to a first current and voltages at the second and third outputs to a second current.

76. A mixer, comprising:

track and hold means for tracking and holding a first signal in response to a second signal; and

limiting means for limiting the response of the track and hold means to a frequency band, the first signal being within the frequency band.

77. The mixer of claim 76 further comprising means for buffering first signal before being applied to the track and hold means.

78. The mixer of claim 76 wherein the track and hold means comprises first and second output signals, the mixer further comprising means for combining the first and second output signals.

79. The mixer of claim 76 wherein the limiting means comprises an inductor and capacitor each being coupled to the track and hold means.

80. The mixer of claim 76 wherein the track and hold means comprises a switch in a path of the first signal, the switch being controlled by the second signal.

81. The mixer of claim 80 wherein the switch comprises a transistor having a gate coupled to the second signal.

82. The mixer of claim 81 wherein the transistor further comprises a source coupled to the first signal.

83. The mixer of claim of 82 wherein the transistor further comprises a drain, and the limiting means comprises a capacitor coupled to the drain.

84. The mixer of claim 83 wherein the limiting means further comprises an inductor coupled to the source of the transistor.

85. The mixer of claim of claim 82 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

86. The mixer of claim of 85 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

87. The mixer of claim 76 wherein the track and hold means comprises a transistor having input means for receiving the first signal and output means for generating an output signal in response to the first signal, and a switch in a path of the output signal, the switch being controlled by the second signal.

88. The mixer of claim 87 wherein the switch comprises a second transistor having a gate coupled to the second signal.

89. The mixer of claim 88 wherein the second transistor further comprises a drain coupled to the output of the transistor.

90. The mixer of claim of 89 wherein the limiting means comprises a capacitor coupled to the output of the transistor.

91. The mixer of claim of 90 wherein the second transistor further comprises a source, and the limiting means further comprises an inductor coupled to the source of the second transistor.

92. The mixer of claim of 89 wherein the second transistor further comprises a source, and the limiting means further comprises an inductor coupled to the source of the second transistor.

93. The mixer of claim of 92 wherein the limiting means comprises a capacitor coupled to the output of the transistor.